

Amendments to the Claims:

Claims 1-162 (canceled)

5 163. (currently amended) A chip package comprising:

~~a silicon substrate;~~

~~a first polymer layer;~~

~~a die between a first portion of said first polymer layer and a second portion of said first polymer layer, wherein said die has a top surface substantially coplanar with a top~~

10 ~~surface of said first portion and with a top surface of said second portion;~~

~~an adhesive material joining a backside of said die to said silicon substrate;~~

~~a first polymer layer on said silicon substrate, wherein said die is in a first opening in said first polymer layer;~~

~~a second polymer layer on said top surface a front side of said die and on said top~~

15 ~~surfaces of said first and second portions; polymer layer;~~

~~a first patterned metal layer over on said second polymer layer, and over said front side top surface of said die and over said top surfaces of said first and second portions, first polymer layer, wherein said first patterned metal layer is connected to said die through a second an opening in said second polymer layer, and wherein said first~~

20 ~~patterned metal layer comprises electroplated copper, and wherein said first patterned metal layer comprises at least a part of a passive device comprising a portion directly over said top surface of said first portion;~~

~~a third polymer layer over on said first patterned metal layer, over said second polymer layer, over said front side top surface of said die and over said top surfaces of~~

25 ~~said first and second portions; and first polymer layer;~~

~~a second patterned metal layer on said third polymer layer, over said front side of said die and over said first polymer layer, wherein said second patterned metal layer is connected to said first patterned metal layer through a third opening in said third polymer~~

~~layer, and wherein said second patterned metal layer comprises electroplated copper; an insulating layer on said second patterned metal layer, on said third polymer layer, over said front side of said die and over said first polymer layer, wherein a fourth opening in said insulating layer is over a pad of said second patterned metal layer and exposes said pad; and~~

5 ~~a metal solder bump over said pad and directly over said top surface of said first portion, polymer layer, wherein said solder metal bump is connected to said pad die through said first patterned metal layer, fourth opening.~~

10 164. (currently amended) The chip package in claim 163, wherein said passive device comprises further comprising a resistor, comprising a portion directly over said first polymer layer.

15 165. (currently amended) The chip package in claim 163, wherein said passive device comprises further comprising a capacitor, comprising a portion directly over said first polymer layer.

166. (previously presented) The chip package in claim 163, wherein said second polymer layer comprises polyimide.

20 167. (previously presented) The chip package in claim 163, wherein said second polymer layer comprises benzocyclobutene (BCB).

25 168. (currently amended) The chip package in claim 163 further comprising a second patterned metal layer on said third polymer layer, over said top surface of said die and over said top surfaces of said first and second portions, wherein said second patterned metal layer comprises electroplated copper, wherein said second patterned metal layer is connected to said first patterned metal layer through an opening in said third polymer

layer, and wherein said metal bump is connected to said first patterned metal layer
through said second patterned metal layer, wherein said die comprises a first contact
point under said second opening and exposed by said second opening, and a second
contact point under a fifth opening in said second polymer layer and exposed by said fifth
5 opening, and wherein said first contact point is connected to said second contact point
through said first patterned metal layer.

169. (previously presented) The chip package in claim 163, wherein said third polymer layer comprises polyimide.

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170. (previously presented) The chip package in claim 163, wherein said third polymer layer comprises benzocyclobutene (BCB).

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171. (currently amended) The chip package in claim 163, wherein said metal bump
comprises a solder, further comprising a passive device over said second polymer layer.

172. (currently amended) The chip package in claim 163, 171, wherein said passive device comprises an inductor, over said second polymer layer.

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173. (currently amended) The chip package in claim 163, 171, wherein said metal bump comprises gold, passive device comprises a capacitor over said second polymer layer.

174. (currently amended) The chip package in claim 163, 171, wherein said passive device comprises a waveguide, resistor over said second polymer layer.

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175. (currently amended) The chip package in claim 163, 171, wherein said passive device comprises a filter, over said second polymer layer.

176. (currently amended) The chip package in claim 163 further comprising a substrate under said die and under said first and second portions, an inductor comprising a portion directly over said first polymer layer.

5 177. (currently amended) The chip package in claim 176, 163 wherein said substrate comprises silicon, further comprising a filter comprising a portion directly over said first polymer layer.

10 178. (currently amended) The chip package in claim 163, wherein said first polymer layer comprises an epoxy.

179. (currently amended) A chip package comprising:

a silicon substrate;

a first polymer layer;

15 a die between a first portion of said first polymer layer and a second portion of said first polymer layer, wherein said die has a top surface substantially coplanar with a top surface of said first portion and with a top surface of said second portion;
an adhesive material joining a backside of said die to said silicon substrate;
a first polymer layer on said silicon substrate, wherein said die is in a first opening in
20 said first polymer layer;

a second polymer layer on said top surface a front side of said die and on said top surfaces of said first and second portions; polymer layer, wherein a second opening in said second polymer layer is over a first pad of said die and exposes said first pad, and a third opening in said second polymer layer is over a second pad of said die and exposes
25 said second pad; and

a patterned metal layer over on said second polymer layer, over said top surface front side of said die and over said top surfaces of said first and second portions, polymer layer, wherein said patterned metal layer comprises electroplated copper, wherein said patterned

metal layer is connected to a said first metal pad of said die through a first opening in said second polymer layer, and to and a second metal pad pads of said die through said a
second opening in said second polymer layer, and third openings, and wherein said first
metal pad is connected to said second metal pad through said patterned metal layer; and -
5 a metal bump directly over said top surface of said first portion, wherein said metal
bump is connected to said die through said patterned metal layer.

180. (currently amended) The chip package in claim 179, wherein said first polymer layer comprises an epoxy.

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181. (currently amended) The chip package in claim 179, wherein said metal bump
comprises a solder, further comprising a capacitor comprising a portion directly over said
first polymer layer.

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182. (previously presented) The chip package in claim 179, wherein said second polymer layer comprises polyimide.

183. (previously presented) The chip package in claim 179, wherein said second polymer layer comprises benzocyclobutene (BCB).

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184. (currently amended) The chip package in claim 179 further comprising a third polymer layer on said patterned metal layer, on over said second polymer layer, over said front side top surface of said die and over said top surfaces of said first and second
portions. polymer layer.

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185. (previously presented) The chip package in claim 184, wherein said third polymer layer comprises polyimide.

186. (previously presented) The chip package in claim 184, wherein said third polymer layer comprises benzocyclobutene (BCB).

187. (currently amended) The chip package in claim 179, wherein said patterned metal layer comprises a ground bus connecting said first and second metal pads through said first and second and third openings.

188. (currently amended) The chip package in claim 179, wherein said patterned metal layer comprises a power bus connecting said first and second metal pads through said first and second and third openings.

189. (currently amended) The chip package in claim 179, wherein said patterned metal layer comprises a signal trace connecting said first and second metal pads through said first and second and third openings.

190. (previously presented) The chip package in claim 179 further comprising a passive device over said second polymer layer.

191. (previously presented) The chip package in claim 190, wherein said passive device comprises an inductor over said second polymer layer.

192. (previously presented) The chip package in claim 190, wherein said passive device comprises a capacitor over said second polymer layer.

193. (previously presented) The chip package in claim 190, wherein said passive device comprises a resistor over said second polymer layer.

194. (currently amended) The chip package in claim 179 further comprising a substrate

under said die and under said first and second portions. solder bump directly over said first polymer layer.

195. (currently amended) The chip package in claim 194, ~~179~~ wherein said substrate 5 comprises silicon, further comprising a gold bump directly over said first polymer layer.

196. (currently amended) The chip package in claim 179, wherein said patterned metal layer comprises electroplated copper, further comprising an inductor comprising a portion directly over said first polymer layer.

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197. (currently amended) A chip package comprising:

15 a substrate;
 a first polymer layer;
 a die between a first portion of said first polymer layer and a second portion of said first polymer layer, wherein said die has a top surface substantially coplanar with a top surface of said first portion and with a top surface of said second portion;
 an adhesive material joining a backside of said die to said substrate;
 a first polymer layer on said substrate, wherein said die is in a first opening in said first polymer layer;
20 a second polymer layer on said top surface a front side of said die and on said top surfaces of said first and second portions; polymer layer, wherein a second opening in said second polymer layer is over a first pad of said die and exposes said first pad, and a third opening in said second polymer layer is over a second pad of said die and exposes said second pad; and
25 a patterned metal layer over on said second polymer layer, over said top surface front side of said die and over said top surfaces of said first and second portions, polymer layer, wherein said patterned metal layer comprises electroplated copper, and wherein said patterned metal layer comprises a ground bus connecting connected to said a first metal

pad of said die through a first opening in said second polymer layer, and to a second metal pad of said die pads through a second opening in said second polymer layer, wherein said first metal pad is connected to said second metal pad through said ground bus; and said second and third openings.

5 a metal bump directly over said top surface of said first portion, wherein said metal bump is connected to said die through said patterned metal layer.

198. (currently amended) The chip package in claim 197 further comprising an inductor over said second polymer layer. comprising a portion directly over said first polymer 10 layer.

199. (currently amended) The chip package in claim 197 further comprising a resistor over said second polymer layer. comprising a portion directly over said first polymer layer.

15 200. (currently amended) The chip package in claim 197, wherein said first polymer layer comprises an epoxy.

201. (currently amended) The chip package in claim 197 further comprising a capacitor over said second polymer layer. comprising a portion directly over said first polymer layer.

202. (previously presented) The chip package in claim 197, wherein said second polymer layer comprises polyimide.

25 203. (previously presented) The chip package in claim 197 further comprising a third polymer layer on said patterned metal layer.

204. (previously presented) The chip package in claim 197, wherein said second polymer layer comprises benzocyclobutene (BCB).

205. (currently amended) The chip package in claim 197, wherein said metal bump comprises further comprising a solder, ~~bump directly over said first polymer layer.~~

206. (currently amended) The chip package in claim 197 further comprising a substrate under said die and under said first and second portions. ~~passive device over said second polymer layer.~~

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207. (currently amended) The chip package in claim 206, wherein said substrate comprises silicon. ~~passive device comprises an inductor over said second polymer layer.~~

208. (currently amended) The chip package in claim 197 206, further comprising a filter over said second polymer layer. ~~wherein said passive device comprises a capacitor over said second polymer layer.~~